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Elektronische Bauelemente

SPW34119D

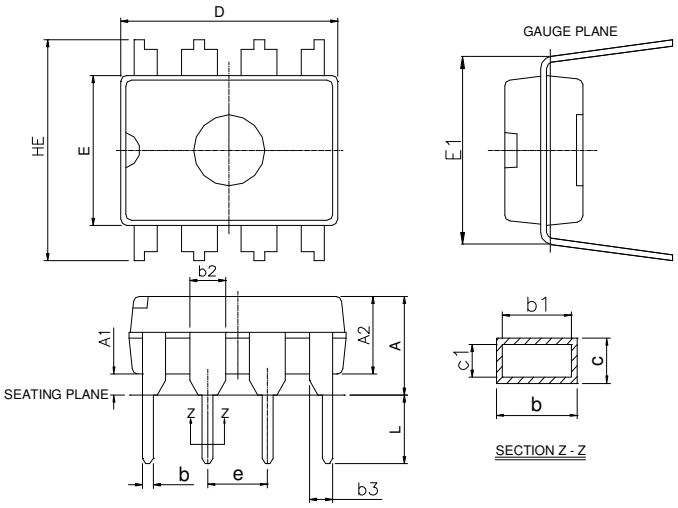
Low Power Audio Amplifier

RoHS Compliant Product

Description

The SPW34119D is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speaker-phones. It provides differential speaker outputs to max. output swing at low supply voltages (2V min.). Coupling capacitors to the speaker are not required. Open loop gain is 80dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal.

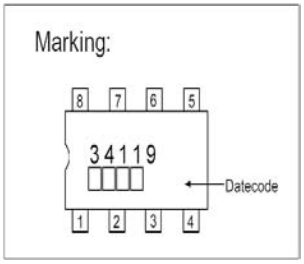
DIP-8



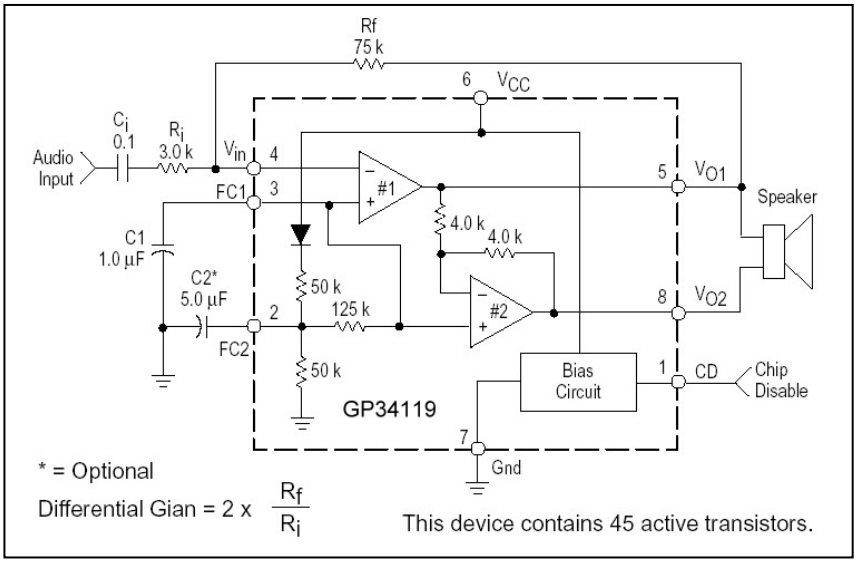
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	-	0.5334	c1	0.203	0.279
A1	0.381	-	D	9.017	10.16
A2	2.921	4.953	E	6.096	7.112
b	0.356	0.559	E1	7.620	8.255
b1	0.356	0.508	e	2.540 BSC	
b2	1.143	1.778	HE	-	10.92
b3	0.762	1.143	L	2.921	3.810
c	0.203	0.356			

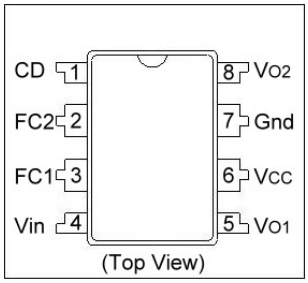
Features

* Output Power Exceeds 250 mW with 32Ω Speaker
* Chip Disable Input To Power Down The IC
* Requires Few External Components
* Drives a Wide Range Of Speaker Loads (8Ω And Up)
* Wide Operating Supply Voltage Range (2V to 16V), Allows Telephone Line Powered Applications
* Gain Adjustable from <0 dB to> 46dB For Voice Band
* Low Quiescent Supply Current (2.7mA Typ) For Battery Powered Applications
* Low Total Harmonic Distortion (0.5% Typ)



Block Diagram and Simplified Application & Pin Configuration





Maximum Ratings

Rating	Value	Unit
Supply Voltage	-1.0 to +18	Vdc
Maximum Output Current at V_{O1}, V_{O2}	±250	mA
Maximum Voltage @ Vin, FC1, FC2, CD Applied Output Voltage to V_{O1}, V_{O2} when disabled	-1.0, V_{CC}+1.0 -1.0, V_{CC}+1.0	Vdc
Junction Temperature	-55, +140	℃

Note: ESD data available upon request.

Recommended Operating Conditions

Characteristics	Symbol	Min	Max	Unit
Supply Voltage Voltage @ CD (Pin 1)	V_{CC} V_{CD}	+2.0 0	+16 V_{CC}	Vdc
Load Impedance	R_L	8.0	-	Ω
Peak Load Current	I_L	-	±200	mA
Differential Gain (5.0kHz Bandwidth)	AVD	0	46	dB
Ambient Temperature	T_A	-20	+70	℃

Pin Function Description

Symbol	Pin	Description
CD	1	Chip Disable-Digital input. A Logic "0" (<0.8V) sets normal operation. A Logic "1" (≧2V) sets the power down mode. Input impedance is nominally 90kΩ.
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog ground for the amplifiers. A 1.0uF capacitor at provides (typically) 52dB of power supply rejection. Turn- capacitor on this pin. This pin can be used as an alternate input.
Vin	4	Amplifier input. This input capacitor a feedback resistor is connected to this pin and V_{O1}.
V_{O1}	5	Amplifier Output #1. The dc level is ≈ (V_{CC} – 0.7)/2.
V_{CC}	6	DC supply voltage (+2V to +16V) is applied to this pin.
GND	7	Ground pin for the entire circuit.
V_{O2}	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out-of-phase with that at V_{O1}. The dc level is ≈ (V_{CC} – 0.7)/2.

Typical Temperature Performance (-20℃ < T_A < +70℃)

Function	Typical Change	Units
Input Bias Current (@ Vin)	±40	pA/℃
Total Harmonic Distortion(V_{CC}=6V, R_L=32Ω Pout=125mW, f=1kHz)	+0.003	%/℃
Power Supply Current (V_{CC}=3V, R_L=∞, CD=0V) (V_{CC}=3V, R_L=∞, CD=2V)	 -0.25 -0.03	uA/℃

Electrical Characteristics (T_A=25℃ unless otherwise noted.)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max.	Unit
Amplifiers (AC Characteristics)						
AC Input Resistance	ri	@ Vin	-	>30	-	MΩ
Open Loop Gain	A_{VOL1}	Amplifier #1, f<100Hz	80	-	-	dB
Close Loop Gain	A_{V2}	Amplifier #2, V_{CC}=6V, f=1kHz, R_L=32Ω	-0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	-	-	1.5	-	MHz
Output Power	P_{Out3} P_{Out6} P_{Out12}	V_{CC}= 3V, R_L= 16Ω, THD ≦ 10% V_{CC}= 6V, R_L= 32Ω, THD ≦ 10% V_{CC}=12V, R_L=100Ω, THD ≦ 10%	55 250 400	- - -	- - -	mW
Total Harmonic Distortion (f=1kHz)	THD	V_{CC}= 6V, R_L=32Ω, P_{out}=125mW V_{CC}≧ 3V, R_L= 8Ω, P_{out}= 20mW V_{CC}≧ 12V, R_L=32Ω, P_{out}=200mW	- - -	0.5 0.5 0.6	1.0 - -	%
Power Supply Rejection (V_{CC}=6V, △V_{CC}=3V)	PSRR	C1=∞, C2=0.01uF C1=0.1uF, C2=0, f=1kHz C1=1.0uF, C2=5.0uF, f=1kHz	50 - -	- 12 52	- - -	dB
Differential Muting	GMT	V_{CC}=6V, 1kHz≦ f ≦ 20kHz, CD=2V	-	>70	-	dB
Amplifiers (DC Characteristics)						
Output DC Level	$V_{O(3)}$ $V_{O(6)}$ $V_{O(12)}$	V_{O1}, V_{O2}, V_{CC}=3V, R_L=16Ω, (R_f=75k) V_{CC}= 6V V_{CC}=12V	1.0 - -	1.15 2.65 5.65	1.25 - -	Vdc
Output Level	V_{OH} V_{OL}	High I_{out}=-75mA, 2V≦V_{CC} ≦ 16V Low I_{out}= 75mA, 2V≦V_{CC} ≦ 16V	- -	V_{CC}-1 0.16	- -	Vdc
Output DC Offset Voltage (V_{O1}-V_{O2})	△V_O	V_{CC} =6V, R_f=75kΩ, R_L=32Ω	-30	0	+30	mV
Input Bias Current	I_{IB}	Vin(V_{CC}=6V)	-	-100	-200	nA
Equivalent Resistance	R_{FC1} R_{FC2}	FC1(V_{CC} =6V) FC2(V_{CC} =6V)	100 18	150 25	220 40	kΩ
Chip Disable(Pin1)						
Input Voltage	V_{IL} V_{IH}	Low High	- 2.0	-	0.8 -	Vdc
Input Resistance	R_{CD}	V_{CC}= V_{CD}=16V	50	90	175	kΩ
Power Supply						
Power Supply Current	I_{CC3} I_{CC16} I_{CCD}	V_{CC}= 3V, R_L=∞, CD=0.8V V_{CC}=16V, R_L=∞, CD=0.8V V_{CC}= 3V, R_L=∞, CD=2.0V	- - -	2.7 3.3 65	4.0 5.0 100	mA mA uA

Note: Currents into a pin are positive, currents out of a pin are negative.

Design Guidelines

General

The SPW34119D is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (V_{O1}-V_{O2}) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

Amplifiers

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier # 1 has an open loop gain of ≧ 80 dB (at f≦ 100 Hz), and the closed loop gain is set by external resistor R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300 Hz to 3400 Hz), a maximum closed loop gain of 46 is recommended. Amplifier #2 is internally set to a gain of-1.0(0dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 V above ground, and to with ≈ 1.3 V below V_{CC}, at the maximum current. See Figures 17 and 18 for V_{OH} and V_{OL} curves.

The output dc offset voltage (V_{O1}-V_{O2}) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers swill generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing V01 to shift negative by an amount equal to [R_f x I_{IB}]. V_{O2} is shifted positive an equal amount. The output offset voltage, specified in the Electrical Characteristics, is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4 to 7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50 k and 125 kΩ resistors. The graph of Figure 1 indicates the turn-on time upon application of V_{CC} of + 6.0 V. The turn-on time is ≈60% longer for V_{CC} = 3.0 V, and ≈20% less for V_{CC} = 9.0V. Turn-off time is < 10 us upon removal of V_{CC}.

Chip Disable

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 V to 0.8 V), the SPW34119D is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 V to V_{CC} V), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0", although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 19.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0 us, and turn on-time is 12 ms-15 ms. Both times are independent of C1,C2, and V_{CC}.

When the SPW34119D is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, V_{O1} and V_{O2}, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

Power Dissipation

Figures 8 to 10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power. The maximum power which can safely be dissipated within the SPW34119D is found from the following equation: $P_D = (140℃ - T_A)/\theta_{JA}$ where T_A is the ambient temperature; and θ_{JA} is the package thermal resistance (100℃/W for the standard DIP package.)

The power dissipated within the SPW34119D, in a given application, is found from the following equation:

$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$ where I_{CC} is obtained from Figure 19; and I_{RMS} is the RMS current at the load; and R_L is the load resistance.

Figures 8 to 10, along with Figures 11 to 13 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the SPW34119D. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0Ω , 16Ω and 32Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the SPW34119D. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25℃. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

Layout Considerations

Normally a snubber is not needed at the output of the SPW34119D, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally, the speaker wires should be twisted tightly, and not more than a few inches in length.

Characteristics Curve

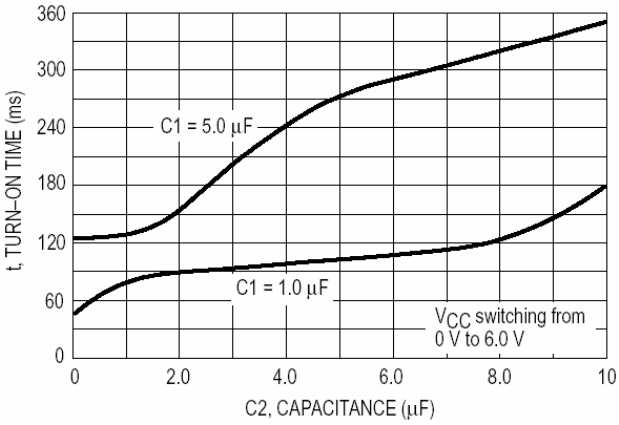


Fig 1. Turn-On Time versus C1, C2 at Power-On

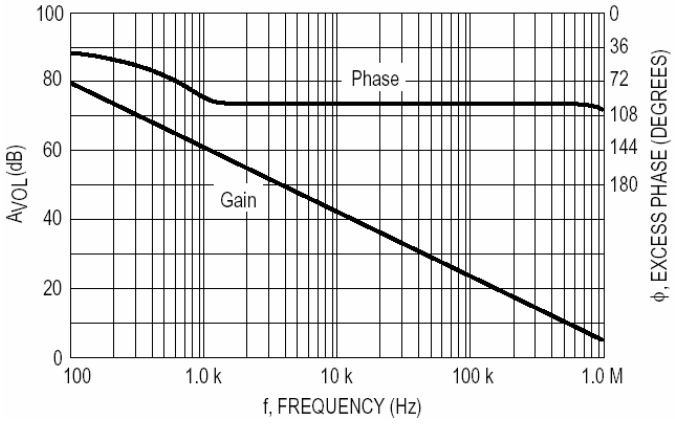


Fig 2. Amplifier #1 Open Loop Gain and Phase

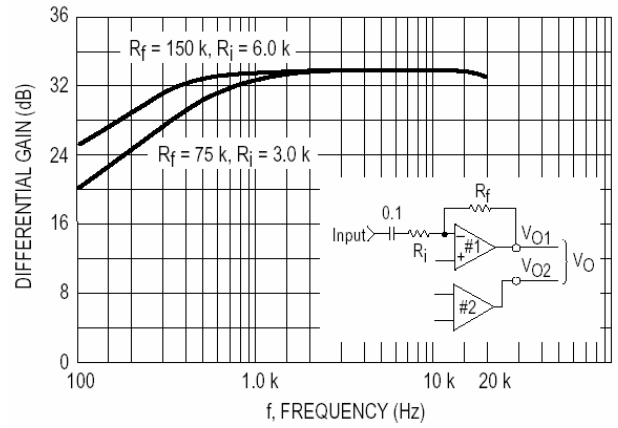


Fig 3. Differential Gain versus Frequency

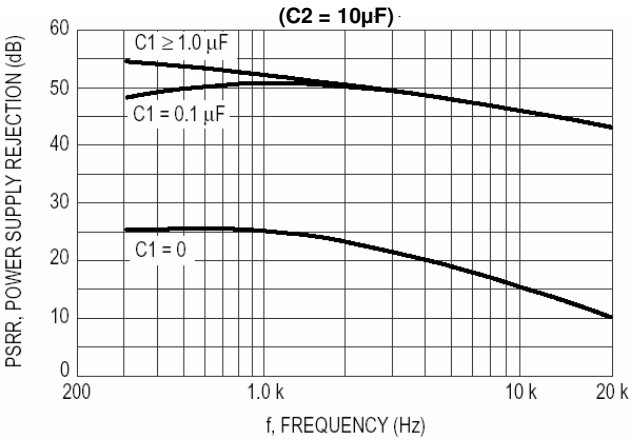


Fig 4. Power Supply Rejection versus Frequency

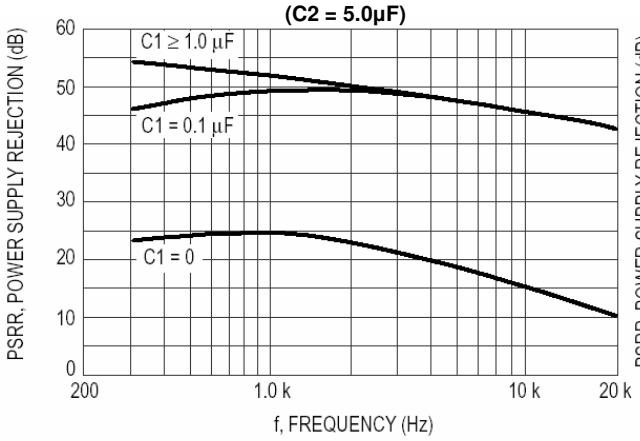


Fig 5. Power Supply Rejection versus Frequency

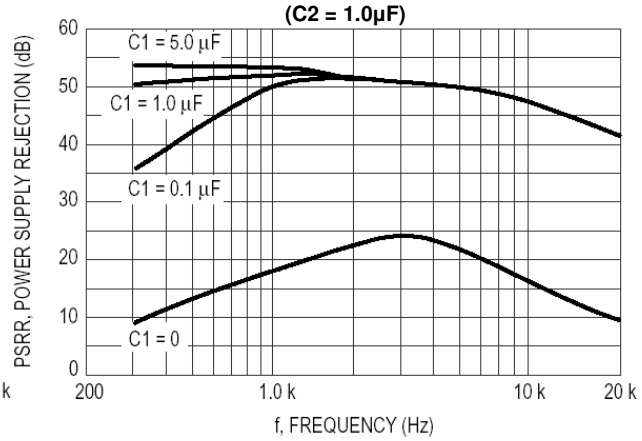


Fig 6. Power Supply Rejection versus Frequency

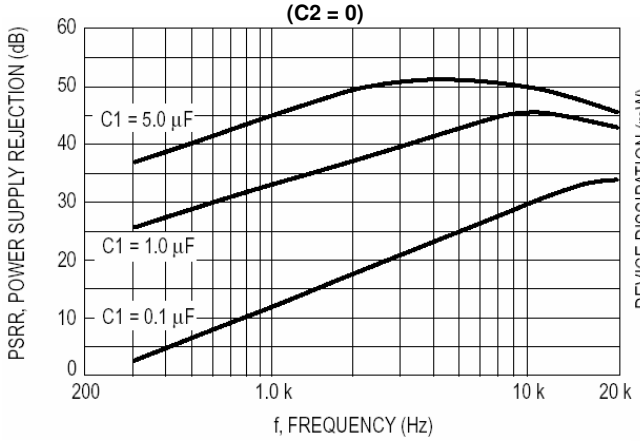


Fig 7. Power Supply Rejection versus Frequency

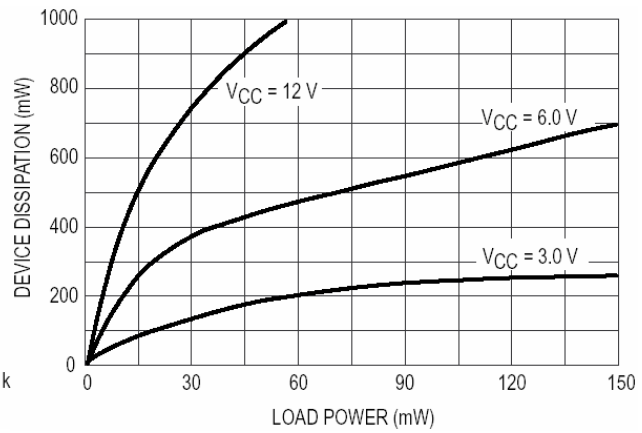


Fig 8. Device Dissipation, 8.0 Ω Load

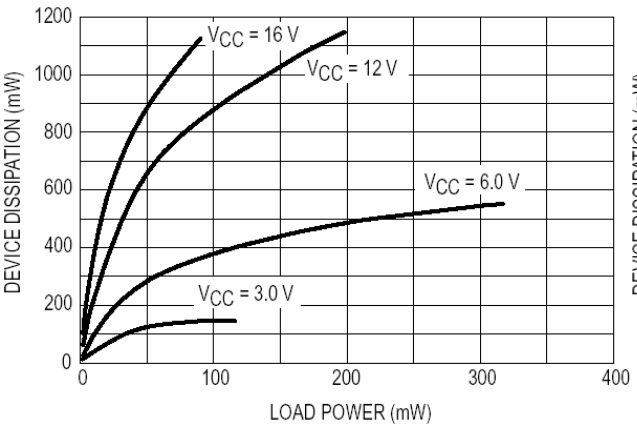


Fig 9. Device Dissipation, 16 Ω Load

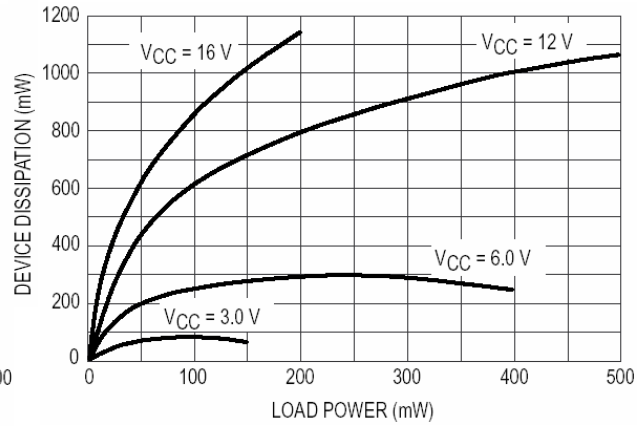


Fig 10. Device Dissipation, 32 Ω Load

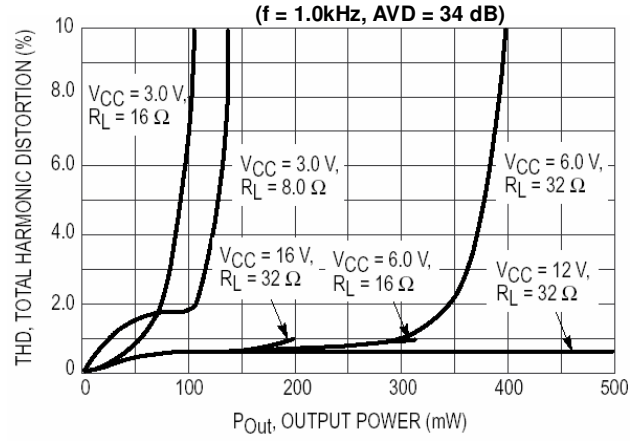


Fig 11. Distortion versus Power

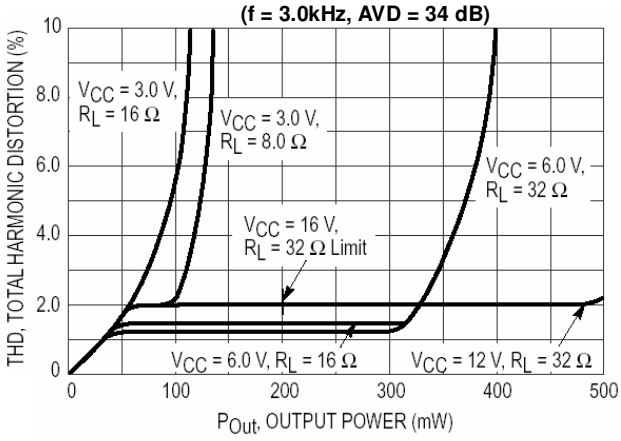


Fig 12. Distortion versus Power

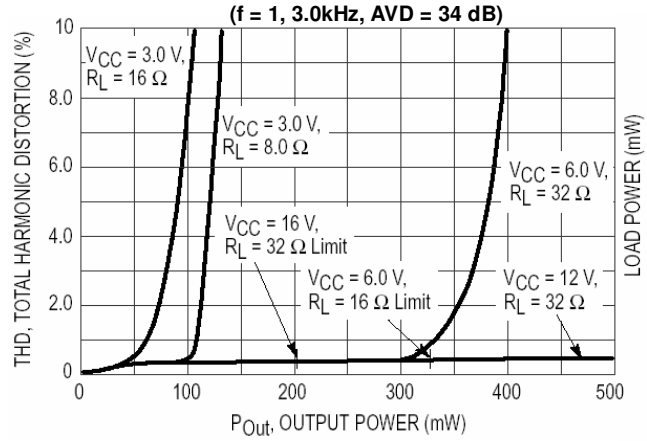


Fig 13. Distortion versus Power

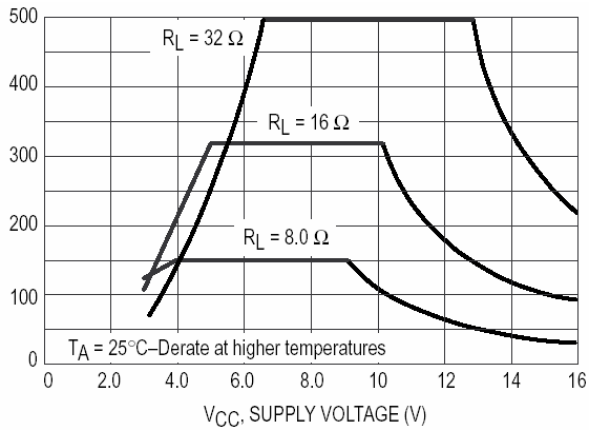


Fig 14. Maximum Allowable Load Power

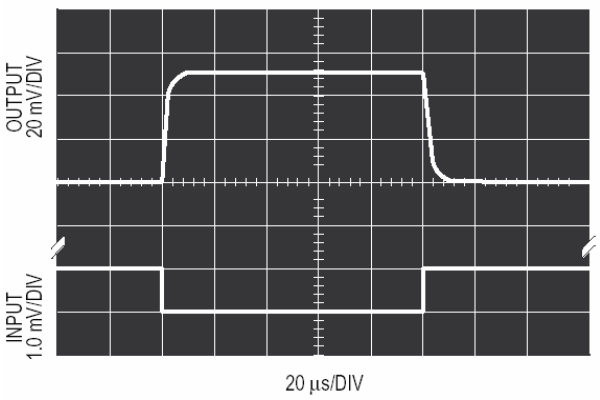


Fig 15. Small Signal Response

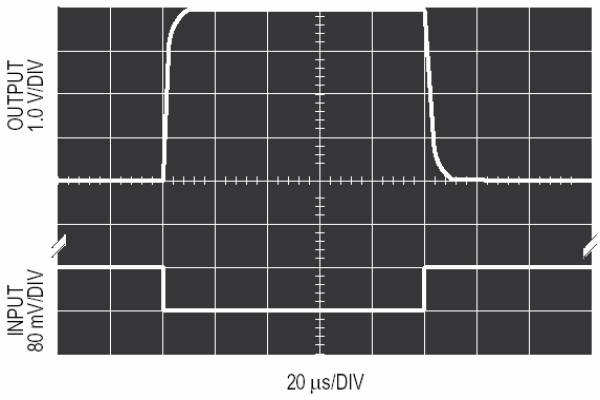


Fig 16. Large Signal Response

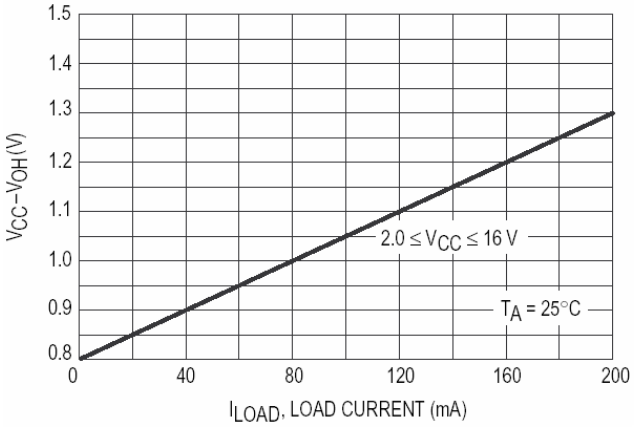


Fig 17. V_{CC}-V_{OH} @ V_{O1}, V_{O2} versus Load Current

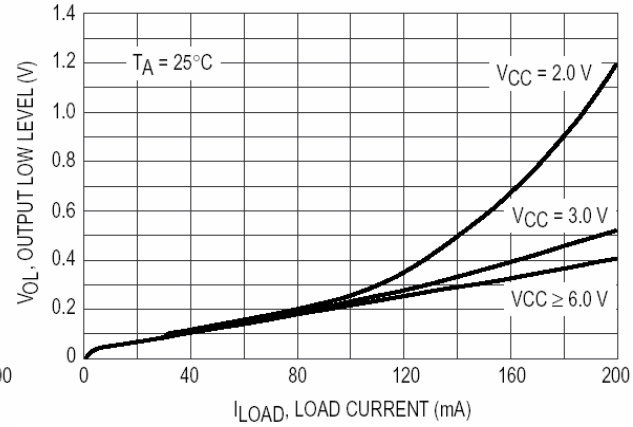


Fig 18. V_{OL} @ V_{O1}, V_{O2} versus Load Current

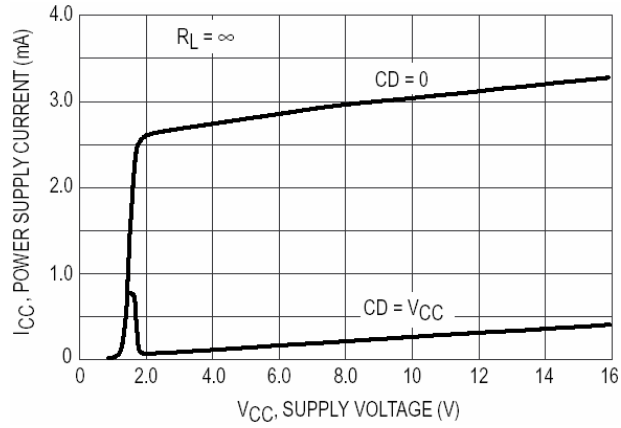


Fig 19. Power Supply Current

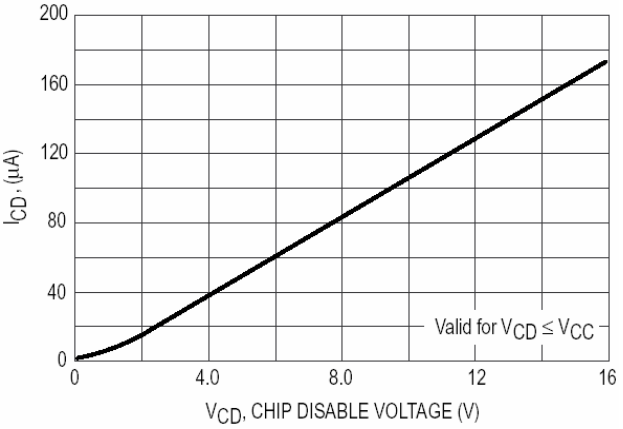


Fig 20. Input Characteristics @ CD (Pin 1)

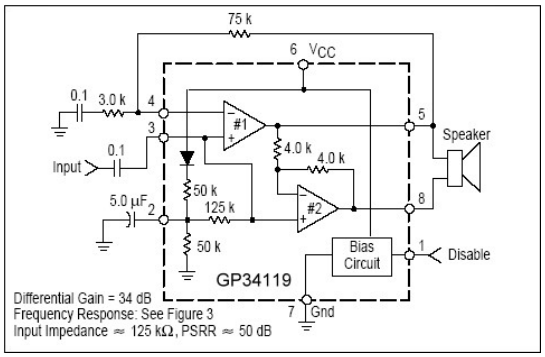
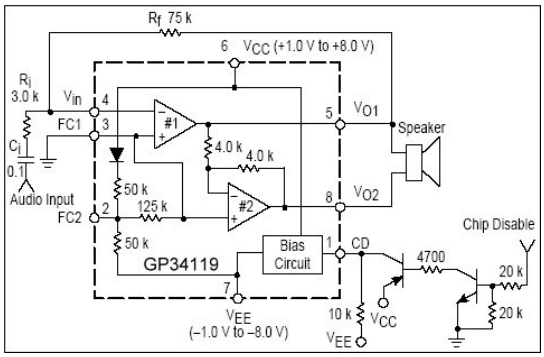


Fig 21. Audio Amplifier with High Input Impedance



Note: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 mist be connected through a capacitor to ground as shown on the front page.

Fig 22. Split Supply Operation

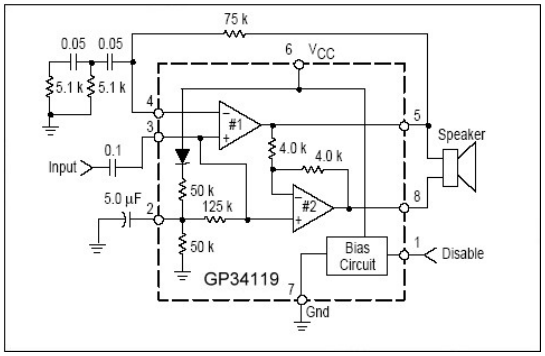


Fig 23. Audio Amplifier with Bass Suppression

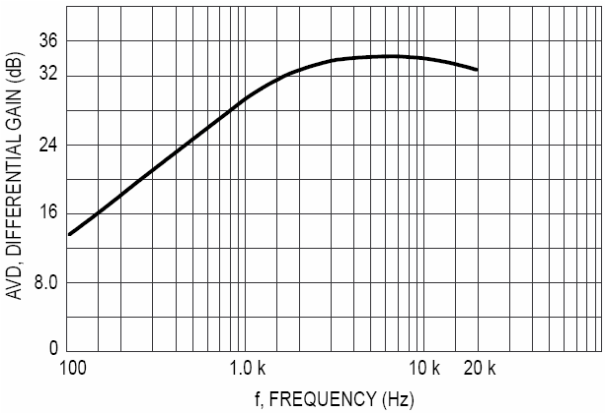


Fig 24. Frequency Response of Fig 23

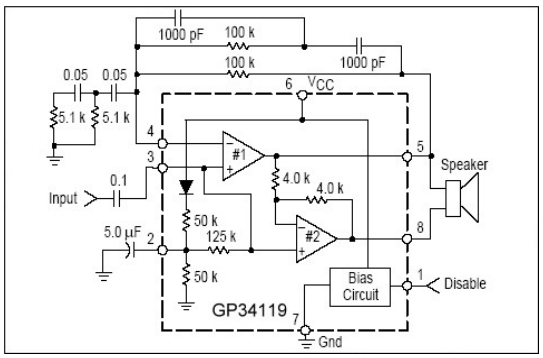


Fig 25. Audio Amplifier with Bandpass

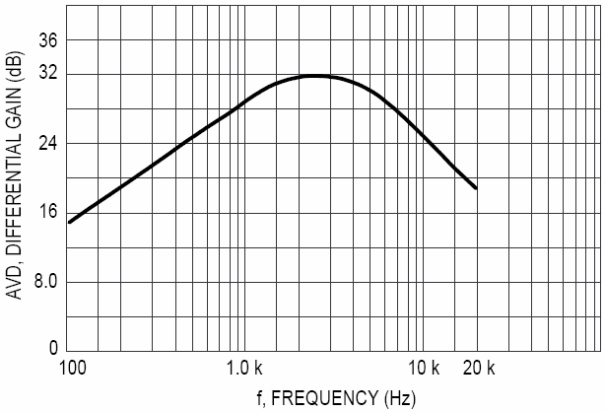


Fig 26. Frequency Response of Fig 25